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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,180	09/26/2003	Jeffrey G. Cheng	00100.03.0032	9865

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EXAMINER	
GUYTON, PHILIP A	

ART UNIT	PAPER NUMBER
2113	

MAIL DATE	DELIVERY MODE
10/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/672,180	CHENG ET AL.	
	Examiner	Art Unit	
	Philip Guyton	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7,9-15,17-19 and 21-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14,15,17-19 and 21-23* is/are allowed.

6)☒ Claim(s) *1,2,5-7,10-13,24-26,28-30 and 32-35* is/are rejected.

7)☒ Claim(s) *4,9,27 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20070823*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 5-7, 10, 11, 24, 25, 26, 28-30, and 32-35 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,742,139 to Forsman et al. (hereinafter Forsman).

With respect to claim 1, Forsman discloses a circuit for monitoring and resetting a co-processor comprising:

a hang detector module operative to detect a hang in the co-processor (column 4, lines 25-27) by detecting a discrepancy between a current state of the co-processor and a current activity of the co-processor (column 4, lines 9-12, lines 25-35); and

a selective processor reset module operative to selectively reset the co-processor without resetting a processor, in response to detecting a hang in the co-processor (column 4, lines 27-35).

With respect to claim 2, Forsman discloses wherein an operating system executes on the processor (column 4, lines 4-5).

With respect to claim 5, Forsman discloses:

a halt communications module operative to halt command communications with the co-processor, in response to detecting a hang in the co-processor (column 5, lines 10-15);

a reset check module operative to detect if the co-processor has been successfully reset, in response to the resetting of the co-processor (column 5, lines 28-33); and

a restart communications module operative to restart command communications with the co-processor, in response to detecting that the co-processor has been successfully reset (column 5, lines 33-35).

With respect to claim 6, Forsman discloses a method of monitoring and resetting a co-processor comprising:

detecting a hang in the co-processor (column 4, lines 25-27) by detecting a discrepancy between a current state of the co-processor and a current activity of the co-processor (column 4, lines 9-12, lines 25-35); and;

selectively resetting the co-processor without resetting a processor, in response

to detecting a hang in the co-processor (column 4, lines 27-35).

With respect to claim 7, Forsman discloses wherein an operating system executes on the processor (column 4, lines 4-5).

With respect to claim 10, Forsman discloses:

halting command communications with the co-processor, in response to detecting a hang in the co-processor (column 5, lines 10-15);

detecting if the co-processor has been successfully reset, in response to the resetting of the co-processor(column 5, lines 28-33); and

restarting command communications with the co-processor, in response to detecting that the co-processor has been successfully reset (column 5, lines 33-35).

With respect to claim 11, Forsman discloses a circuit for monitoring and resetting a co-processor comprising:

a hang detector module operative to detect a hang in the co-processor (column 4 lines 25-27);

a halt communications module operative to halt executable instruction communications with the co-processor, in response to detecting a hang in the co-processor (column 5, lines 10-15);

a selective processor reset module operative to selectively reset the co-processor without resetting a processor, in response to detecting a hang in the co-processor (column 4, lines 27-35);

a reset check module operative to detect if the co-processor has been successfully reset, in response to the resetting of the co-processor (column 5, lines 28-33); and

a restart communications module operative to restart executable instruction communications with the co-processor, in response to detecting that the co-processor has been successfully reset (column 5, lines 33-35).

With respect to claim 24, Forsman discloses a memory containing instructions executable on a processor that causes the processor to:

detect a hang in a co-processor (column 4, lines 25-27) by detecting a discrepancy between a current state of the co-processor and a current activity of the co-processor (column 4, lines 9-12, lines 25-35); and

selectively reset the co-processor without resetting the processor, in response to detecting a hang in the co-processor (column 4, lines 27-35).

With respect to claim 25, Forsman discloses instructions that causes the processor to detect if the co-processor has been successfully reset, in response to the resetting of the co-processor (column 5, lines 28-33).

With respect to claim 26, Forsman discloses a circuit for monitoring and resetting a co-processor comprising:

a hang detector module operative to detect a hang in the co-processor (column 4, lines 25-27) by detecting a discrepancy between a current state of the co-processor and data in one or more storage elements associated with the co-processor, wherein the data in the one or more storage elements represents a current activity of the co-processor (column 4, lines 9-12, lines 25-45); and

a selective processor reset module operative to selectively reset the co-processor without resetting a processor, in response to detecting a hang in the co-processor (column 4, lines 27-35).

With respect to claim 28, Forsman discloses wherein the hang detector module is operative to determine if the data in the one or more storage elements reflects processing of instructions by the co-processor (column 4, lines 36-45).

With respect to claim 29, Forsman discloses wherein the current state of the co-processor is represented by data stored in the one or more storage elements associated with the co-processor (column 4, lines 36-45).

With respect to claim 30, Forsman discloses a method of monitoring and resetting a co-processor comprising:

detecting a hang in the co-processor (column 4, lines 25-27) by detecting a discrepancy between a current state of the co-processor and data in one or more storage elements associated with the co-processor, wherein the data in the one or more storage elements represents a current activity of the co-processor (column 4, lines 9-12, lines 25-45); and

selectively resetting the co-processor without resetting a processor, in response to detecting a hang in the co-processor (column 4, lines 27-35).

With respect to claim 32, Forsman discloses determining if the data in the one or more storage elements reflects processing of instructions by the co-processor (column 4, lines 36-45).

With respect to claim 33, Forsman discloses wherein the current state of the co-processor is represented by data stored in the one or more storage elements associated with the co-processor (column 4, lines 36-45).

With respect to claim 34, Forsman discloses a memory containing instructions executable on a processor that causes the processor to:

detect a hang in a co-processor (column 4, lines 25-27) by detecting a discrepancy between a current state of the co-processor and data in one or more storage elements associated with the co-processor, wherein the data in the one

or more storage elements represents a current activity of the co-processor (column 4, lines 9-12, lines 25-45); and

selectively reset the co-processor without resetting the processor, in response to detecting a hang in the co-processor (column 4, lines 27-35).

With respect to claim 35, Forsman discloses wherein the discrepancy is detected by comparing data representing a current state of the co-processor (column 4, lines 36-50) with data representing a current activity of the co-processor (column 4, lines 25-35).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forsman in view of U.S. Patent App. No. 2002/0093505 to Hill et al. (hereinafter Hill).

With respect to claim 12, Forsman does not disclose expressly wherein the processor is a host processor and the co-processor is a graphics processor.

Hill discloses a system in which a graphics processor works with the main CPU to execute graphic-intensive software (paragraph 21 - graphics processor referred to as "graphic accelerator"). Hill's system prevents the entire computing

system from crashing due to a failure specific to the graphics accelerator, by performing a series of tests (paragraph 23, lines 1-16). If the graphics accelerator does not perform adequately, the software graphics processor will take over instead of crashing the system (paragraph 34, last 4 lines, paragraph 35). Hill discloses that he intends to improve situations where a reset due to a graphics processor crash is unacceptable (paragraph 19, last 8 lines). Forsman also wishes to recover a system of multiple processors without performing a full system reset (Forsman - column 1, lines 25-29). Using a graphics processor in place of a service processor in Forsman's system would prevent system crashes due to graphics accelerators as well as the service processor, preventing crashes due to incompatible video accelerators or other faults. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the graphics accelerator monitoring system of Hill into the processor reset system of Forsman, providing additional protection against hardware failure.

With respect to claim 13, Forsman discloses wherein the hang detector module detects the hang in the graphics processor by detecting a discrepancy between a current state of the graphics processor and a current activity of the graphics processor (column 4, lines 9-12, lines 25-35).

Response to Arguments

5. Applicant's arguments filed 27 August 2007 with regard to claims 1-2, 5-7, 10-13, 24-26, 28-30, and 32-35 have been fully considered but they are not persuasive.

With regard to claims 1, 6, and 24, applicant argues that Forsman does not disclose a system that detects a discrepancy between a current state of the co-processor and a current activity of the co-processor. The examiner respectfully disagrees. The cited portions of Forsman disclose a system in which a host processor and a service processor exchange heartbeat signals (column 4, lines 9-12). The heartbeat signals indicate that a service processor is active and working correctly (column 1, lines 35-37). In other words, the heartbeat signal is an indication of the current activity of the processor. In order for an abnormality to be found, the status of the service processor must be normal (column 4, lines 36-45). Thus, a discrepancy exists, and the host resets the service processor and returns it to its original state and activity where it can continue to process heartbeat signals (column 4, lines 46-50).

Applicant again argues that the heartbeat signal is not capable of indicating a discrepancy. More particularly, applicant states that the heartbeat signal is capable of indicating only one of two things: functioning or not functioning, and at best indicates either current state or current activity of the processor, but not both. In contrast, applicant argues that the current invention requires more. However, the examiner maintains that the claims only require detection of a discrepancy. There is no requirement in the claims that the current

state and the current activity are detected. Thus, there are only two states – discrepancy or no discrepancy, that the claimed invention detects. And, in fact, new claim 35 recites language in which current state and current activity are detected, and therefore illustrates the differences in the limitations.

Furthermore, in Forsman, the absence of heartbeat signals does not automatically indicate a service processor failure, as the status register may indicate an exceptional condition (column 4, lines 36-45). Thus, applicant's interpretation that at the time of failure to detect heartbeat signals the current state of the processor is not active and working correctly is incorrect. Instead, the current state is actually determined by status of the service processor at the moment that failure of heartbeat signal detection occurs.

Regarding claims 26, 30, and 34, applicant further asserts that checking of the status/control register occurs after it has been determined that the service processor is not functioning correctly, and is therefore not performed in the process of detecting a hang. However, this is not correct. Forsman teaches wherein the status/control register is checked after a failure to detect heartbeat signals (column 4, lines 36-45). If no status exceptions are present, then the processor is reset (column 4, lines 46-50). Examples of status exceptions include when the service processor is in a special debug mode or when the service processor is in the process of handling a critical event (column 4, lines 40-44). Both of these are indications that the service processor is not in a hang condition. Thus, checking of the status register is part of the detection of a hang in the service processor.

With regard to claim 11, applicant argues that Forsman does not disclose a halt communications module operative to halt command communications with the co-processor, in response to detecting a hang in the co-processor. The examiner respectfully disagrees. Applicant asserts that the disclosure of waiting a predetermined timeout period for the service processor to respond to a reset warning signal does not teach halting of command communications with the co-processor, because communication is possible. However, the examiner maintains that this is an incorrect interpretation of the claim. In Forsman, although communication is possible, during the period that the host is waiting for acknowledgement, communication has been halted (column 5, lines 10-22 and figure 3, steps 304-308). In this period of time that the host is waiting, whether an acknowledgement is received or the process times-out, there is not other communication between the host and the service processor. Thus, all communications, including executable instruction communications are halted.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is

filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Philip Guyton whose telephone number is (571) 272-3807. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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